WHAT IS CLAIMED IS:

1. A semiconductor device including n-channel field-effect transistors and p-channel field-effect transistors formed on a semiconductor substrate, wherein:

the transistors are disposed with a gate electrode and a source and a drain corresponding thereto;

a direction joining the source and the drain is formed in a direction along a <100> crystal axis or an axis equivalent to the <100> crystal axis; and

compression strain is formed in which crystal strain of channel portions of the p-channel field-effect transistors is greater than crystal strain of channel portions of the n-channel field-effect transistors.

2. A semiconductor device including n-channel field-effect transistors and p-channel field-effect transistors formed on a semiconductor substrate, wherein:

the transistors are disposed with a gate electrode and a source and a drain corresponding thereto;

a direction joining the source and the drain is formed in a direction along a <100> crystal axis or an axis equivalent to the <100> crystal axis; and

tensile strain is formed in which crystal strain of channel portions of the n-channel field-effect transistors is greater than crystal strain of channel portions of the p-channel field-effect transistors.

3. A semiconductor device including a semiconductor substrate, a gate electrode and a plurality of transistor formed on the semiconductor substrate, the plurality of transistor disposed with a drain and a source corresponding to the gate electrode, an insulating film formed above the transistors, with a direction joining the source and the corresponding drain of the transistors being formed in a direction along a <100> crystal axis or an axis equivalent to the <100> crystal axis,

the transistors including a plurality of n-channel field-effect transistor and plurality of p-channel field-effect transistor,

the insulating film including tensile stress,

the insulating film that is formed in regions at the peripheries of the p-channel field-effect transistors and positioned in directions parallel and orthogonal to the direction joining the source and the drain including an insulating film that is thinner than the insulating film that is formed in regions at the peripheries of the n-channel field-effect transistors and positioned in directions parallel and orthogonal to the direction joining the source and the drain.

4. The semiconductor device of claim 3, further including an interlayer insulating film including an upper end above the insulating film and a wiring layer above the interlayer insulating film.

5. A semiconductor device including a semiconductor

substrate, a plurality of active region enclosed by field regions formed on the semiconductor substrate, a gate electrode and a plurality of transistor formed on the active regions, the a plurality of transistor disposed with a drain and a source corresponding to the gate electrode, an insulating film formed above the transistors, with a direction joining the source and the corresponding drain of the transistors being formed in a direction along a <100> crystal axis or an axis equivalent to the <100> crystal axis,

the transistors including a plurality of n-channel field-effect transistor and a plurality of p-channel field-effect transistor corresponding to the n-channel field-effect transistors,

the insulating film including tensile stress,

wherein the insulating film that is thinner than the insulating film formed at regions positioned between the first n-channel field-effect transistors and the second n-channel field-effect transistors is formed on or not disposed on field regions adjacent to the active regions formed by the p-channel field-effect transistors.

6. A semiconductor device including n-channel field-effect transistors and p-channel field-effect transistors formed on a silicon substrate,

wherein the n-channel field-effect transistors and the p-channel field-effect transistors are plurally included,

a direction in which drain currents of the transistors mainly flow is a direction along a <100> crystal axis or an axis equivalent to the <100> crystal axis,

an insulating film including tensile stress is formed at upper portions of the n-channel field-effect transistors and the p-channel field-effect transistors, and

the insulating film that is thinner than the insulating film formed at regions positioned between first n-channel field-effect transistors and second n-channel field-effect transistors is formed on or not disposed on field regions adjacent to active regions of the p-channel field-effect transistors.

7. A semiconductor device including a semiconductor substrate, a gate electrode and a plurality of transistor formed on the semiconductor substrate, the plurality of transistor disposed with a drain and a source corresponding to the gate electrode, an insulating film formed above the transistors, with a direction joining the source and the corresponding drain of the transistors being formed in a direction along a <100> crystal axis or an axis equivalent to the <100> crystal axis,

the transistors including a plurality of n-channel field-effect transistor and a plurality of p-channel field-effect transistor,

the insulating film including compression stress,

the insulating film that is formed in regions at the

peripheries of the n-channel field-effect transistors and positioned in directions parallel and orthogonal to the direction joining the source and the drain including an insulating film that is thinner than the insulating film that is formed in regions at the peripheries of the p-channel field-effect transistors and positioned in directions parallel and orthogonal to the direction joining the source and the drain.

8. A semiconductor device including a semiconductor substrate, a plurality of active region enclosed by field regions formed on the semiconductor substrate, a gate electrode and a plurality of transistor formed on the active regions, the plurality of transistor disposed with a drain and a source corresponding to the gate electrode, an insulating film formed above the transistors, with a direction joining the source and the corresponding drain of the transistors being formed in a direction along a <100> crystal axis or an axis equivalent to the <100> crystal axis,

the transistors including a plurality of n-channel field-effect transistor and a plurality of p-channel field-effect transistor,

the insulating film including compression stress,

wherein the insulating film that is thinner than the insulating film formed at regions positioned between first p-channel field-effect transistors and second p-channel field-effect transistors is formed on or not disposed on field

regions adjacent to the active regions of the n-channel field-effect transistors.

9. A semiconductor device including a plurality of active region enclosed by field regions formed on a silicon substrate and n-channel field-effect transistors and p-channel field-effect transistors formed in the active regions,

wherein the n-channel field-effect transistors and the p-channel field-effect transistors are plurally included,

a direction in which drain currents of the transistors mainly flow is a direction along a <100> crystal axis or an axis equivalent to the <100> crystal axis, an insulating film including compression stress is formed at upper portions of the n-channel field-effect transistors and the p-channel field-effect transistors, and

the insulating film that is thinner than the insulating film formed at regions positioned between first p-channel field-effect transistors and second p-channel field-effect transistors is formed on or not disposed on field regions adjacent to active regions of the n-channel field-effect transistors.

10. A semiconductor device including a semiconductor substrate, element forming regions plurally disposed on the semiconductor substrate via element isolating regions, a gate electrode formed on the element forming regions, a plurality of transistor disposed with a drain and a source corresponding

to the gate electrode, an insulating film formed above the transistors, with a direction joining the source and the corresponding drain of the transistors being formed in a direction along a <100> crystal axis or an axis equivalent to the <100> crystal axis,

the transistors including a plurality of n-channel field-effect transistor and a plurality of p-channel field-effect transistor, and

a trench width of the element isolating regions adjacent to regions at which the p-channel field-effect transistors are formed is narrower than a trench width of the element isolating regions adjacent to the n-channel field-effect transistors.

11. The semiconductor device of claim 10, wherein the trench width of the element isolating regions that are adjacent to regions at which the p-channel field-effect transistors are formed and positioned in directions parallel and orthogonal to the direction joining the source and the drain is narrower than the trench width of the element isolating regions that are adjacent to regions at which the n-channel field-effect transistors are formed and positioned in directions parallel and orthogonal to the direction joining the source and the drain.

12. The semiconductor device of claims 1 to 11, wherein the Raman shift of Raman spectrometry when a laser is irradiated onto channel portions of the n-channel field-effect transistors is smaller than the Raman shift of Raman spectrometry when a

laser is irradiated onto channel portions of the p-channel field-effect transistors.

13. The semiconductor device of claims 1 to 11, wherein the insulating film includes silicon nitride as a main component.

14. A method of manufacturing a semiconductor device, the method comprising the steps of:

forming, on a semiconductor substrate, n-channel field-effect transistors and p-channel field-effect transistors disposed with a gate electrode and a drain and a source corresponding to the gate electrode;

depositing a stress control film so as to cover the field-effect transistors;

depositing and patterning a mask above the stress control film;

etching the stress control film;

depositing an interlayer insulating film after depositing the stress control film; and

forming, above the interlayer insulating film, a wiring layer that electrically communicates with the transistors,

wherein a direction that joins the source and the drain is formed in a direction along a <100> crystal axis or an axis equivalent to the <100> crystal axis,

tensility or compression strain is made to reside in the stress control film, and channel portions of the p-channel field-effect transistors in directions parallel and orthogonal

to the direction joining the source and the drain are formed so as to include compression strain that is larger than that of channel portions of the n-channel field-effect transistors in directions parallel and orthogonal to the direction joining the source and the drain.

15. The method of manufacturing a semiconductor device of claim 14, wherein the etching removes the stress control film from regions forming contact plugs and removes or makes at peripheries of the p-channel field-effect transistors the stress control film thinner than peripheries of the n-channel field-effect transistors.

16. A semiconductor device including a semiconductor substrate, a gate electrode and a plurality of transistor formed on the semiconductor substrate, the transistors disposed with a drain and a source corresponding to the gate electrode, and a plurality of circuit disposed with the transistors,

wherein a first circuit is disposed with a first transistor and a second circuit is disposed with a second transistor,

a direction joining a corresponding drain and a source configuring the first transistor of the first circuit is formed in a direction along a <100> crystal axis of the substrate or an axis equivalent to the <100> crystal axis, and

a direction joining a corresponding drain and a source configuring the second transistor of the second circuit is formed in a direction along the <100> crystal axis of the substrate

or an axis equivalent to the <100> crystal axis.